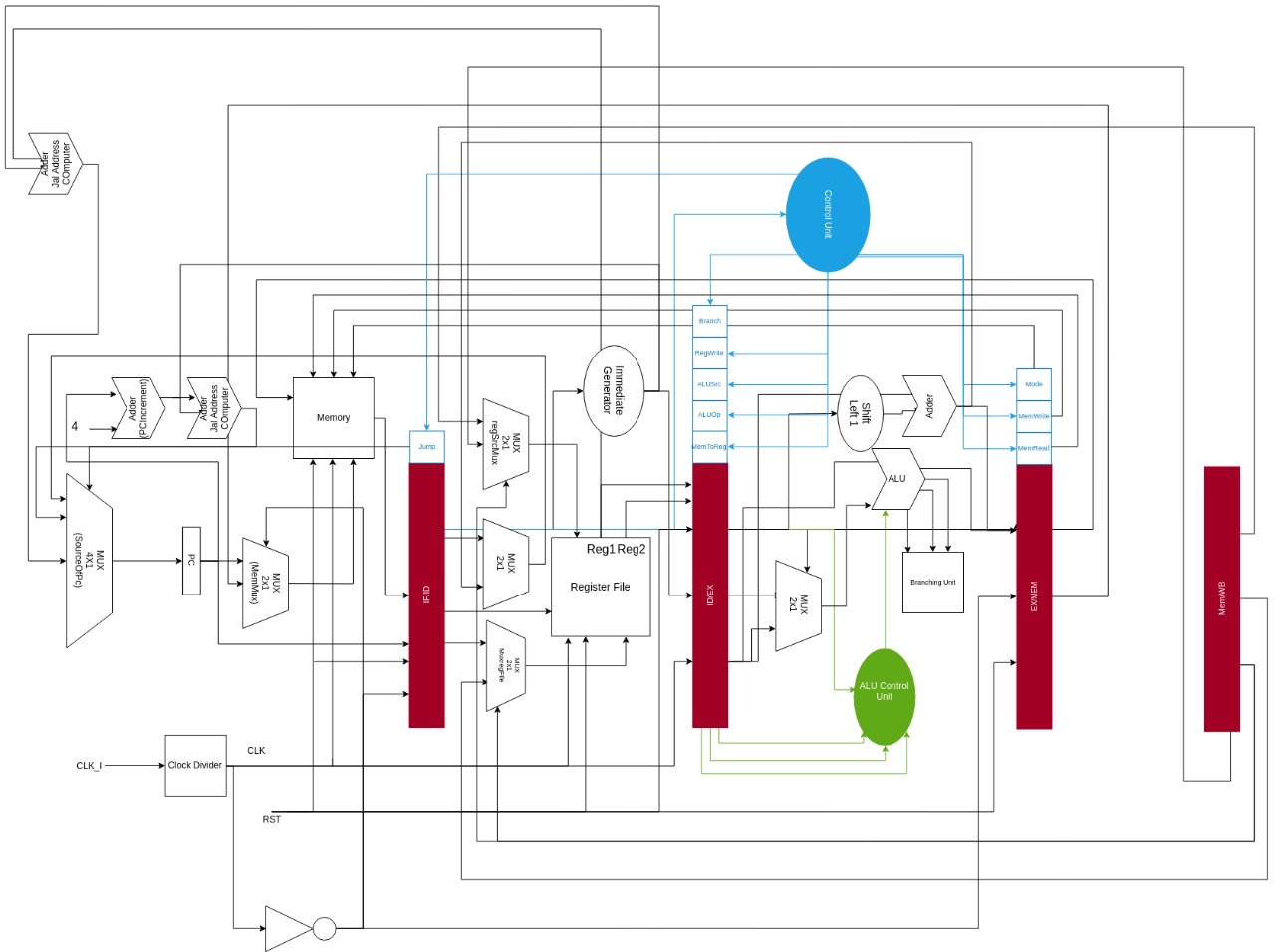
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**Project 1 MS1**

**Computer Architecture**



1. FETCH

The fetching stage is where the program counter sends the address of the instruction to be fetched via a MUX choosing between the pc address or the address of the data to be written in the memory.

This arises the problem of the single ported memory: we solved this problem with the MUX mentioned above.

Finally, all the needed values for the instruction are saved in the IF\_ID pipeline register.

1. DECODE

This stage is where we decode the instruction via the control unit, which gives the CPU components what to execute, and by reading the register file values if needed. We also generate the relevant instruction immediate used by the instruction if any.

1. EXECUTE

This stage is where the actual instruction executes via the ALU and identifying if any branch must be taken and take it if needed.

1. MEMORY

This stage writes or loads data from the memory.

1. WRITE BACK

This stage writes the result from the ALU in the register if needed.

To know our logging, see our issues on github: https://github.com/djzenma/RV32IC-CPU